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|  | NBKR INSTITUTE OF SCIENCE & TECHNOLOGY :: VIDYANAGAR  LESSON PLAN FORM  Form no: TEA/04/00 |

Department : **ELECTRONICS & COMMUNICATION ENGINEERING – B Section**

Academic Year : 2016-2017

Class : III B.Tech. II Semester

Subject : **DIGITAL DESIGN**

Faculty Name : **Sri M Raveendra**

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| **Sl. No.** | | **Description of Topic** | **No. of Periods** | | **Dates** | |
| **Planned** | **Taken** | |  |
|  | | UNIT – I |  |  | |  |
|  | | **MOS Amplifiers:** |  |  | |  |
| 1 | | Common source amplifier with resistive load | 2 |  | |  |
| 2 | | Common Drain amplifier | 2 |  | |  |
| 3 | | Differential amplifier | 3 |  | |  |
| 4 | | transfer characteristics and derivation of CMRR | 2 |  | |  |
|  | | **Current Mirrors:** |  |  | |  |
| 5 | | Basic Current Mirrors | 1 |  | |  |
| 6 | | cascode current mirror and active current mirrors without signal analysis | 3 |  | |  |
|  | |  |  |  | |  |
|  | | UNIT – II |  |  | |  |
|  | | Digital Integrated circuits: |  |  | |  |
| 1. | | Evaluation of ICs | 1 |  | |  |
| 2. | | Advantages and classification of ICs. | 1 |  | |  |
| 3. | | Digital IC characteristics, | 1 |  | |  |
| 4. | | Digital IC families- DTL, HTL | 1 |  | |  |
| 5. | | ECL | 1 |  | |  |
| 6. | | MOS & CMOS | 2 |  | |  |
| 7. | | TTL-Totem-pole, Open collector and Tristate outputs and IC packaging’s | 3 |  | |  |
|  | **UNIT – III** | |  |  | |  |
|  | | **VHDL introduction and language fundamentals:** |  |  | |  |
| 1. | | VHDL History – Design methodology: - Description style | 2 |  | |  |
| 2. | | Direction of design, design flow, step in digital system design | 3 |  | |  |
| 3. | | Hardware modeling issue: concurrency, delays, delta time and back annotation | 3 |  | |  |
| 4. | | organization of a VHDL design file – libraries | 1 |  | |  |

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| 5. | Language fundamentals: Basic sequential statements – Date types – Assignment statements and, | 2 | |  |  |
| 6. | operators – Objects in VHDL: Signals, Variable, constants, files-attributes of objects – VHDL package | 3 | |  |  |
| 7. | package body and configurations – Entity declarations and statements – Examples of simple circuits | 2 | |  |  |
|  | UNIT – IV |  | |  |  |
|  | **Combinational circuit building blocks:** |  | |  |  |
| 1. | Multiplexes | 2 | |  |  |
| 2. | Decoders | 1 | |  |  |
| 3. | Encoders | 1 | |  |  |
| 4. | Code converters & their implémentation using VHDL | 2 | |  |  |
|  | UNIT – V |  | |  |  |
|  | **Sequential logic design:** |  | |  |  |
| 1. | Latches and flip-flops | 3 | |  |  |
| 2. | Registers, counters (Asynchronous and synchronous) BCD | 2 | |  |  |
| 3. | Ring and Johnson counter and their implementation usingVHDL | 2 | |  |  |
|  | Total : | **52** | |  |  |

Date: Faculty Signature

HOD Signature